## Amendments to the Claims

1. *(Currently Amended)* . A method ~~(100)~~ for detecting delay faults in a semiconductor memory comprising:

providing ~~(110, 120)~~ address bits and data bits according to a test pattern suitable for testing the semiconductor memory;

providing ~~(130)~~ the address bits and the data bits to input ports of the semiconductor memory; and,

starting ~~(140, 150)~~ memory operation in dependence upon the address bits, wherein a time interval between the provision of the address bits and the data bits and the start of the memory operation is approximately equal to an operating clock cycle of the semiconductor memory.

2. *(Original)* A method for detecting delay faults in a semiconductor memory as recited in claim 1 wherein providing address bits and data bits includes:

generating address bits and data bits; and,

validating the address bits and the data bits prior to providing same to the input ports of the semiconductor memory.

3. *(Original)* A method for detecting delay faults in a semiconductor memory as recited in claim 1 wherein the memory operation comprises writing the data bits into the semiconductor memory.

4. *(Currently Amended)* A method for detecting delay faults in a semiconductor memory as recited in claim 3 wherein the memory operation comprises reading ~~(160)~~ data bits out of the semiconductor memory.

5. *(Original)* A method for detecting delay faults in a semiconductor memory as recited in claim 4 further comprising:

repeating the steps according to the test pattern.

6. *(Currently Amended)* A method for detecting delay faults in a semiconductor memory as recited in claim 5 further comprising:

comparing ~~(170)~~ read out data with predetermined data to obtain at least a comparison result; and,

if the at least a comparison result is indicative of a match providing a signal indicating that the semiconductor memory is fault free.

7. *(Original)* A method for detecting delay faults in a semiconductor memory as recited in claim 6 wherein the time interval is determined by appropriate timing of the address and data validation.

8. *(Original)* A method for detecting delay faults in a semiconductor memory as recited in claim 6 wherein the time interval is determined by appropriate timing of the start of the memory operation.

9. *(Original)* A method for detecting delay faults in a semiconductor memory as recited in claim 6 wherein the test pattern is a March test.

10. *(Original)* A method for detecting delay faults in a semiconductor memory comprising:

providing valid address bits and data bits according to a test pattern suitable for testing the semiconductor memory;

providing the valid address bits and the valid data bits to input ports of the semiconductor memory;

writing the valid data bits into the semiconductor memory in dependence upon the valid address bits, wherein a time interval between the provision of the valid address bits and the valid data bits and start of the write operation is approximately equal to an operating clock cycle of the semiconductor memory;

providing second valid address bits according to the test pattern;

providing the second valid address bits to the input ports of the semiconductor memory;

reading second data bits out of the semiconductor memory in dependence upon the second valid address bits, wherein a time interval between the provision of the second valid address bits and start of the read operation is approximately equal to an operating clock cycle of the semiconductor memory; and,

comparing the second data bits with predetermined data to obtain a comparison result and if the comparison result is indicative of a match indicating that the operation was fault free.

11. *(Original)* A method for detecting delay faults in a semiconductor memory as recited in claim 10 wherein providing valid address bits and valid data bits includes:

generating address bits and data bits; and,

validating the address bits and the data bits to provide the valid address bits and the valid data bits; and,

wherein providing second valid address bits includes:

generating second address bits according to the test pattern;

validating the second address bits to provide second valid address bits.

12. *(Original)* A method for detecting delay faults in a semiconductor memory as recited in claim 10 comprising:

repeating the steps according to the test pattern.

13. *(Original)* A method for detecting delay faults in a semiconductor memory as recited in claim 12 wherein the test pattern is a march test.

14. *(Original)* A method for detecting delay faults in a semiconductor memory as recited in claim 13 wherein the time interval is determined by appropriate timing of the address and data validation.

15. *(Original)* A method for detecting delay faults in a semiconductor memory as recited in claim 13 wherein the time interval is determined by appropriate timing of the start of the memory operation.

16. *(Original)* A test circuitry for detecting delay faults in a semiconductor memory comprising:

address and data generating circuitry for generating address bits and data bits according to a test pattern suitable for testing the semiconductor memory;

connecting circuitry in communication with the semiconductor memory for providing the address bits and the data bits to the semiconductor memory; and,

timing circuitry for providing a time signal for timing the provision of the address bits and the data bits and start of the memory operation such that a time interval between the provision of the address bits and the data bits and the start of the memory operation is approximately equal to an operating clock cycle of the semiconductor memory.

17. *(Original)* A test circuitry for detecting delay faults in a semiconductor memory as recited in claim 16 comprising:

validation circuitry for validating the address bits and the data bits.

18. *(Original)* A test circuitry for detecting delay faults in a semiconductor memory as recited in claim 16 comprising comparison circuitry for comparing read out data with predetermined data to obtain a comparison result and if the comparison result is indicative of a match indicating that the operation was fault free.

19. *(Original)* A test circuitry for detecting delay faults in a semiconductor memory as recited in claim 18 wherein the address and data generating circuitry, the validation circuitry, the connecting circuitry, the timing circuitry, and the comparison circuitry are integrated within a chip comprising the semiconductor memory.